CLAIMS

1. (Cancelled)

2. (Cancelled)

3. (Previously presented) A semiconductor memory device, comprising:

a first plurality of pads to receive a corresponding plurality of first external signals;

a second plurality of pads to receive a corresponding plurality of second external signals; and

an input and output mode set circuit coupled with the first and second plurality of pads to generate a plurality of input and output mode signals responsive to the plurality of first and second external signals;

wherein, during a test mode, the input and output mode set circuit is adapted to generate the plurality of input and output mode signals responsive only to the plurality of first external signals, the plurality of first pads receiving a high voltage higher than a voltage level of a power supply signal thereby generating a plurality of first external signals having a level higher than a voltage level of the power supply signal;

wherein, during normal operations, the input and output mode set circuit is adapted to generate the plurality of input and output mode signals responsive to the plurality of second external signals, the plurality of second external signals having logic levels.

4. (Cancelled)

5. (Currently amended) The semiconductor memory device of claim 3 wherein the power supply signal is applied to the semiconductor memory device after the high voltage is applied to one of the first plurality of pads.

6. (Original) The semiconductor memory device of claim 3 wherein the plurality second pads float.

7. (Original) The semiconductor memory device of claim 3 wherein at least one of the plurality of second pads is grounded to a ground terminal of the semiconductor memory device.

8. (Previously presented) The semiconductor memory device of claim 3 wherein the input and output mode set circuit comprises:

a pad circuit coupled with the first plurality of pads, to generate a plurality of first signals, one of the plurality of first signals being active when the high voltage is applied to at least one of the first plurality of pads;

a control signal generating circuit to generate a plurality of control signals responsive to the plurality of first signals and a plurality of second signals; and

an input and output mode signal generating circuit to generate the plurality of input and output mode signals responsive to the plurality of control signals and the plurality of second external signals.

9. (Original) The semiconductor memory device of claim 8 wherein the plurality of second signals comprises a power supply sense signal activated when the power supply signal has a level equal to or greater than a predetermined level and input and output mode control signal activate responsive to a write enable signal, a row address strobe signal, and a column address strobe signal.

10. (Previously presented) A semiconductor memory device, comprising:

a plurality of pads for receiving a corresponding plurality of external signals; and

an input and output mode set circuit coupled with the plurality of pads, to generate a plurality of input and output mode signals;

wherein, during a test mode, the input and output mode set circuit is adapted to generate the plurality of input and output mode signals responsive to a plurality of mode register address signals; and

wherein, during normal operation, the input and output mode set circuit is adapted to generate the plurality of input and output mode signals responsive to the plurality of external signals received at the plurality of pads.

11. (Original) The semiconductor memory device of claim 10 wherein each of the plurality of pads float.

12. (Original) The semiconductor memory device of claim 11 wherein at least one of the plurality of pads is grounded.

13. (Cancelled)

14. (Previously presented) The semiconductor memory device of claim 20 wherein the first internal signal is a power supply sense signal enabled when a power supply has a level equal to or greater than a predetermined level and the second internal signals is enabled when a write enable signal, a row address strobe signal, and a column address strobe signal are enabled.

15. (Previously presented) The semiconductor memory device of claim 20 wherein, during the normal operation, the second mode register signal and the first and second internal signals are deactivated thereby deactivating the first, second, and third control signals and wherein the input and output mode signal generating circuit is adapted to generate the input and output mode signals responsive to the plurality of external signals

16. (Original) The semiconductor memory device of claim 10 wherein the plurality of pads includes two pads.

17. (Cancelled)

18. (Cancelled)

19. (Previously presented) The semiconductor memory device of claim 3 wherein the high voltage is applied to the plurality of first pads only for a short period of time.

20. (Previously presented) The semiconductor memory device of claim 10 wherein the input and output mode set circuit comprises:

a mode register set circuit to receive a group of the plurality of mode register address signals and first and second internal signals and to generate first and second mode register signals responsive to the group of mode register address signals and the first and second internal signals;

a control signal generating circuit to generate a plurality of control signals responsive to the first and second mode register signals, a remaining group of the plurality of mode register address signals, the first internal signal, and a third internal signal; and

an input and output mode signal generator to receive the plurality of control signals, cut off signals the plurality of external control signals responsive to at least one of the plurality of control signals, and generate the plurality of input and output mode signals responsive to the remaining control signals.